Technical Note

1965-42

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et al.

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Target Simulator

17 September 1965

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Lexington, Massachusetts
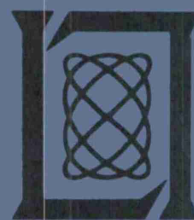
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

THE DATA RECOVERY CENTER TARGET SIMULATOR

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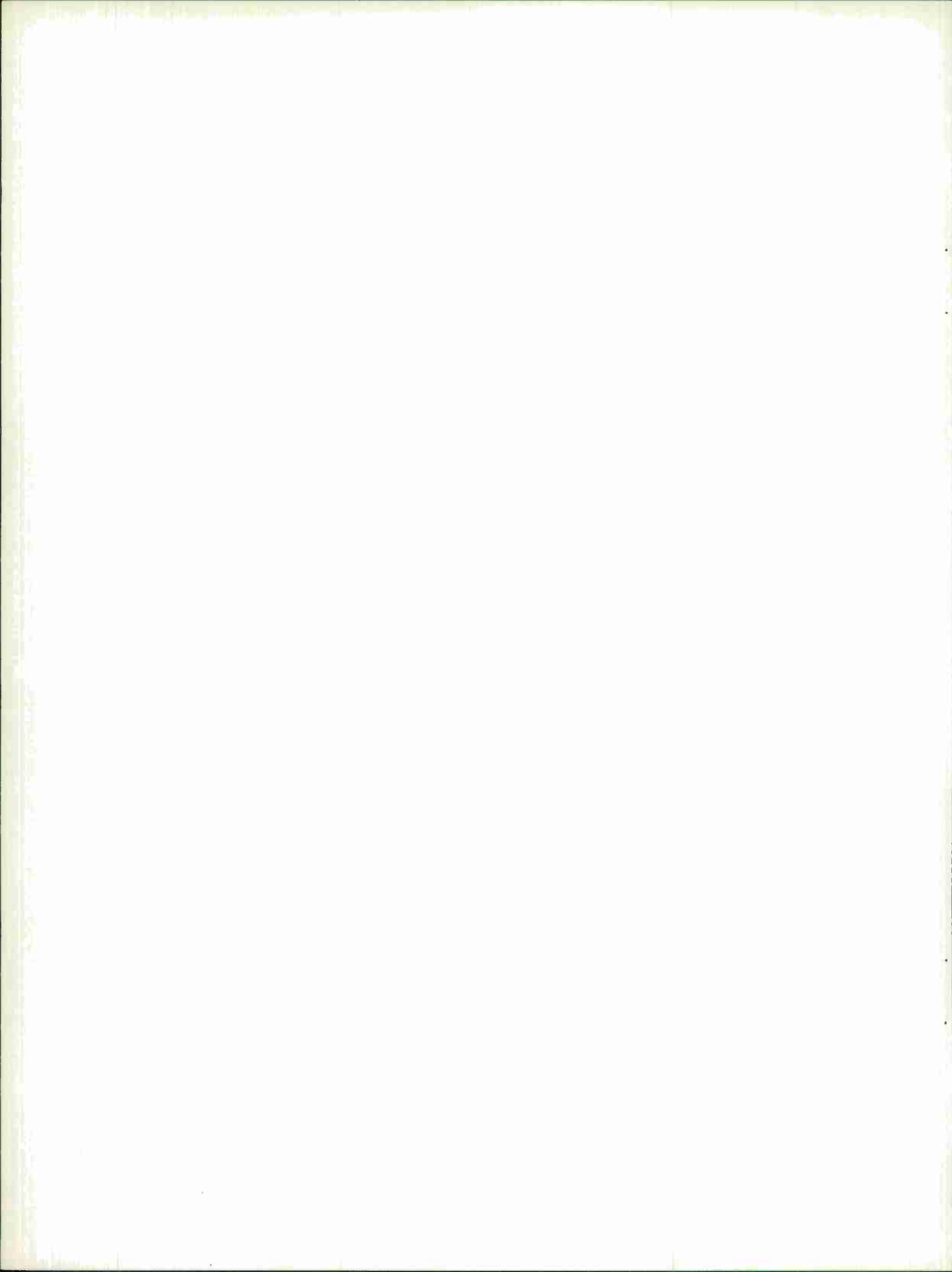*D. BUZZARD*

Radio Corporation of America

TECHNICAL NOTE 1965-42

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LEXINGTON   MASSACHUSETTS

ABSTRACT

It is very important for the operation of the Lincoln Data Recovery Center to be able to inject into it artificially generated targets. These target-pulses must simulate as closely as possible those appearing in the input from the I. F. tape into the D. R. C. and should be controllable in range, width, amplitude, phase and repetition rate by special computer programs written for the CDC-3200 computer. In addition to the FM channels of the tape, its digital channels must be simulated.

A target simulator has been constructed to the above specifications and is described in the text.

TABLE OF CONTENTS

THE DATA RECOVERY CENTER
TARGET SIMULATOR

I.   INTRODUCTION

In the course of the preparations for the installation and operation of the TRADEX Data Recovery Center*(DRC) it became clear that it would be of great importance to be able to generate targets artificially for injection into the DRC.   These targets would have to simulate as closely as possible the input coming from an I. F. tape into the DRC but would be controllable in range, width, amplitude, phase and repetition rate by digital signals coming off the CDC 3200 computer and would be generated in turn by special programs.   The integration of the simulator with the computer will permit great speed and flexibility in all the applications.   This Data Recovery Center Target Simulator (DRCTS) was consequently built by the staff and technicians of Group 21[†] and became operational in April 1965.

The uses of the DRCTS are of three types:

        a)   Checkout and trouble shooting for the DRC system,

        b)   alignment of the DRC and its subsystems, and

        c)   performance measurements and/or calibrations.

The flexibility necessary to carry out these functions is achieved by the use of the CDC 3200 computer and a set of programs which will be designed for the above functions.   It is envisaged to write the programs in modular form so that larger test programs can be formed from them by hooking several of them together.   Also, they will contain a number of input-parameters making easy variation of tests feasible.

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* O. V. Fortier and P. J. Harris, G-1964-24, "A Short Description of the TRADEX Data Recovery System, " (5 May 1964).

† The staff mainly involved in the design and implementation were A. H. Flink, O. V. Fortier, J. H. Halberstein, P. J. Harris, R. M. Martinson, E. J. Peters, K. E. Ralston and D. F. Sedivec of Lincoln Laboratory and D. Buzzard of RCA.

Since the DRCTS should be useable as a secondary standard for calibration of the DRC receiver and SDS, its precision with respect to amplitude, phase, range and pulse width is designed to exceed that of the DRC system itself.

A. General Description of the Target Simulator

Of the 15 tracks on the I. F. tape, ten contain FM signals corresponding to the output of ten I. F. channels of the TRADEX receiver:

L-band	L. C.	normal gain	
L-band	R. C.	normal gain	
L-band	L. C.	fixed gain	
L- band	L. C.	fixed gain	
UHF	L. C.	normal gain	reference
UHF	R. C.	normal gain	reference
UHF	L. C.	fixed gain	reference
UHF	R. C.	fixed gain	reference
UHF	L. C.		azimuth error
UHF	L. C.		elevation error

After discrimination in the DRC playback unit these channels give the corresponding I. F. signals at 375 kHz[*]. A target would correspond to an I. F. pulse delayed from the main pulse by the time corresponding to its range. The Target Simulator will therefore generate pulses of 375 kHz; their amplitude, phase, width and range will be computer controlled. The simulated signals will represent the output of any of the ten IF-channels. The corresponding simulator channels are Channels 1 and 2 (Fig. 1). There will be two more FM channels on the tape carrying CW reference signals for L-band and UHF. Either one of the CW references will be simulated, the corresponding output appearing on Channel 3 (Fig. 1).

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[*] The 1.5 MHz TRADEX I. F. transforms to 375 kHz because of the 4:1 reduction in DRC playback speed.

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The remaining three of the fifteen tape tracks are for "direct" channels, i. e., they are not frequency modulated. Of these channels, only two have to be simulated, namely the digital data channel (Channel 4 in Fig. 1) and the $5.12/4 = 1.28$ MHz range clock (Channel 5 in Fig. 1). The generation of the digital data channels is described in detail in Section B.

A block diagram of the Target Simulator and its connections to the DRC is given in Fig. 1. The DRCTS and the computer are connected through a 3707 data channel. This channel transmits and/or receives 24 bits of data in parallel and requires a data transmitter, receiver and transmission line. The data received in the simulator are stored in storage registers until used. A more detailed description of the data links is given in Section A.

Since the Target Simulator circuits, the computer and the DRC were procured from independent sources their logic levels are different and level converters had to be used in the interfaces (block 2, Fig. 1).

A 5.12 MHz stable oscillator is counted down to $5.12/4$ MHz to account for the 4:1 reduction in DRC playback speed and shaped and adjusted in level to simulate the $5.12/4$ MHz range clock track of the I.F. tape (block 3, Fig. 1).

The phase shifter uses as inputs a stable 355 kHz osicllator and the 5.12 MHz clock counted down to 20 kHz. The 20 kHz signal is shifted in phase by a digital phase signal and mixed with the 355 kHz to form a phase shifted signal at 375 kHz. A second not phase shifted signal of 375 kHz is produced and serves as a reference (block 5, Fig. 1).

The phase shifted signals are formed into pulses by a pulse gate which is computer controlled through the pulse range and pulse width controls (blocks 6, 7 and 8, Fig. 1). The resulting pulses pass through digitally controlled attenuators (block 9, Fig. 1). The digital phase shifter is described in detail in Section C-2. The generation of the target pulses is described in Sections C-1 through C-3 and the binary attenuator in Section C-4.

The characteristics of the simulator are summarized in Table I below:

TABLE I

	Minimum Step	Range of Variation	Number of Bits in Computer Message
Pulse Range	190 ft = 1/32 mi	(0 - 256) mi	13
Pulse Width	190 ft = 1/32 mi	$(0-50)\mu$sec = (0-6140) ft	6
Amplitude	1/4 db	(0 - 63-3/4) db	8
Phase	1.4063°	$(0^{\circ} - 360^{\circ})$	8
PRF (in miles)	1 mi	(0 - 256) mi	8

II. DETAILED DESCRIPTION OF THE TARGET SIMULATOR

A. Computer-Simulator Interface Logic

The computer-simulator interface logic (Fig. 2) ensures that the data generated by the computer arrive at the simulator at the proper time and go to the correct locations. The data lines carrying the data are connected to the CDC 3200 by the CDC 3207 data channel. In order to start the transmit cycle an interrupt pulse (Sect. B-2) is sent from the simulator to the computer and serves as a ready-signal. When the computer has data to transmit after receiving the interrupt pulse, a connect line goes high and the 3-bit connect-code assigned to the simulator appears on the three connect-code lines. The arrival of the data signal and the state of the connect-code lines are sensed by logic blocks 1 through 4 in Fig. 2, and the flip-flop CS (Connect Store, block 5) is set or reset when the connect-code is correct or incorrect, respectively. CS enables or disables the AND gate 6 and with it the connection between the computer and simulator. The pulse from block 4 is also necessary to trigger a pulse on the reply line to the computer (out of block 17). The computer then clears the connect line and connect-code lines; the data signal line goes high and the data appear on the data lines. This data can now be loaded into the appropriate registers by applying load clock pulses d_4 (Sect. B-1) to block 6. The word counter in blocks 8, 9, and 10 counts the number of words loaded; the loading signals are enabling pulses from the lines labelled "load 1", "load 2", etc., to the data register transfer matrices (Fig. 5). After allowing sufficient time for loading each word (through the multivibrator in block 17) a pulse is sent on the reply line permitting loading of a new word. After having sent 5 words the computer program stops sending data words until a new interrupt pulse is received from the simulator. When "load 5" has been executed a reset pulse R from block 18 resets the word counter restoring the system to its initial state. A new interrupt pulse will restart the cycle. During each cycle the simulator transmits six replies and receives five data signals. The total load time for all five words, which includes the built-in delays, is 60 µsec. The connect code lines are time shared and used as data

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lines after the computer-simulator connection has been established. The connection from block 7 to block 6 ensures that no new signals can enter through block 6 while block 7 is true and no new data can be sent by the computer to the signal lines before the previous word has been loaded.

B. Digital Data Track (Figs. 3, 4, 5)

As mentioned briefly in the introduction there is a digital data track on the DRC I. F. tape containing 6.25 μsec pulses at 1 mile ≅ 50 μsec intervals, a synchronization pulse about 25 μsec long, and 72 data bits (3 computer words) which appear in a sequence as shown in Fig. 3. The pre-zero gate extends from the trailing edge of the -7-mile mark to the trailing edge of the zero-mile mark. The digital data gate extends from there to the trailing edge of the 18-mile mark. The positions of the 72 bits are indicated in Fig. 3; there are four bit-positions per mile. The range marks are omitted in the pre-zero gate and digital data gate except for the -1-mile and zero-mile marks. In order to simulate the digital data track, the 72 data bits are assembled by the computer in three 24-bit digital data words in the format shown in Fig. 4a. This format corresponds to the format of the 72 bits in the digital data track if read out sequentially. The computer transmits two more 24-bit words, the target designation words (Fig. 4b), to the simulator in order to designate the range, amplitude, width, and phase of the simulated pulse as well as the maximum radar-range in miles corresponding to the PRF. We shall refer to this range as "PRF in miles."

The five words are transmitted from the computer to their registers in the simulator by means of a 3207 data channel. The control of this channel is accomplished by the computer-simulator interface logic which was described in Section A-1. The registers (Fig. 5) for the digital data words are shift registers which are loaded from the data lines when the command pulses "load 1", "load 2", and "load 3" appear at the input of the transfer matrices (blocks 11 through 14) which multiply them logically with the bit levels on the data lines. The 72 bits and spares are then shifted in the correct sequence through the shift register (blocks 1 through 9) by pulses from the shift clock $f(d_6)$ (Fig. 8).

1. Generation of the Timing Pulses (Fig. 6)

The one mile range marks are generated from a signal of a 5.1224375 MHz oscillator; the 5.12 MHz signal is counted down by a factor of 256 and anded as shown in Fig. 6. The pulses obtained are 49.9762076 μsec apart which corresponds to one TRADEX-mile[*] in the DRC. The 5.12/4 MHz clock pulse derived from block 4 of Fig. 6 simulates the timing Channel 5 (Fig. 1) recorded on the IF tape. The signals d_3, d_4 and d_6 are used in other parts of the simulator.

2. Generation of the Interrupt Pulses (Fig. 7)

The interrupt pulse is the one mile range mark occurring 7 miles before zero time (Fig. 3). The PRF in miles register is loaded when the "load 4" command is received from the data circuits connect logic. The register is connected as a counter which is disabled by the flip-flop I_0 during the loading time. Specifically, as will be seen below, I_0 is true from the falling edge of the -7-mile mark to the falling edge of the zero-mile mark. The PRF in miles counter can start counting down when $\overline{I_0}$ is true and on the trailing edge of the next mile mark i.e., the 1-mile mark.

The PRF counter is set to the number (PRF in miles minus n) on the trailing edge of the n-mile mark. On the PRF in miles minus 8 mark it is set to -8. On the next mile mark namely the -7-mile mark, the AND gate of block 1 in Fig. 7 is enabled and its output, which coincides with the -7-mile mark, serves as the interrupt pulse. On the trailing edge of the interrupt pulse the flip-flop I_0 goes true and the pre-zero counter S_1, S_2, S_3 is set to binary 111 = decimal 7. On the -6-mile mark the pre-zero counter counts down to 6 etc. On the trailing edge of the -1-mile mark the AND gate of block 2 is enabled and on the trailing edge of the next mile mark,the zero mile mark,I_0 goes false. Thus the I_0 flip-flop marks the pre-zero gate as indicated above.

3. Generation of the Gated d_6-Pulses and the Gated One Mile Marks (Fig. 8)

The digital data formatting register (Fig. 5) is shifted by pulses called f (d_6). These are 6.25 μsec pulses spaced 12.5 μsec apart which appear only during the

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[*] A TRADEX-mile equals 6142.0 feet.

digital data gate (Fig. 3). The generation of $f(d_6)$ is shown in Fig. 8. The data gate counter is counted up by the range marks starting from the 1-mile mark. On the trailing edge of the 18-mile range mark $J_1 \cdot \overline{J}_2 \cdot \overline{J}_3 \cdot \overline{J}_4 \cdot J_5$ goes from true to false and resets the flip-flop β, so that flip-flop β is true from the trailing edge of the zero-range mark to the trailing edge of the 18-mile range mark. Hence we obtain the pulses of $f(d_6)$ in the output of the multiplier.

As shown in Fig. 3 all the one-mile marks have to appear in the digital data track except those at -6 through -2 miles and those at 1 through 18 miles. These gated range marks are generated as shown in Fig. 8. The flip-flop I_{18} in the figure is flipped when either I_0 or $S_1 \cdot S_2 \cdot \overline{S}_3$ goes from true to false. Moreover, it is set by the trailing edge of the interrupt pulse and reset by the trailing edge of the 18-mile range mark. Hence the gate I_{18} is closed by the interrupt pulse and is opened again when $S_1 \cdot S_2 \cdot \overline{S}_3$ goes false at the trailing edge of the -2-mile range mark, is closed when I_0 goes false at the trailing edge of the zero-range mark and is opened again by the trailing edge of the 18-mile range mark. Anding the output of the gate I_{18} with the range marks gives the required gated one-mile range marks.

C. Generation of the Target Pulses

In addition to the digital data words the computer transmits two control words to the simulator which determine the range, width, amplitude and phase of the pulse and the "PRF in miles, " which is the number of radar miles between two main pulses at the PRF given. We have seen the generation of the interrupt pulses, the pre-zero gate and the digital word gate in the previous sections.

1. Target Gate Generation (Fig. 9 and Fig. 1, blocks 6 through 9)

The target range register (Fig. 9a) is loaded from the computer data lines when the "load 4"-pulse is received from the data circuits connect logic (Fig. 2). The register is connected as a counter which is disabled during the loading time, when I_0 is true. After $\overline{I}_0$ becomes true on the falling edge of the zero range mark the counter will start counting on the trailing edge of the d_3-pulse. Since the d_3-pulses are 1/32 of a mile apart, the smallest range increment in the simulator is 189. 944 ft.

When the range counter is down to zero and $\overline{I}_0 = 1$, the variable P_0 (Fig. 9b) becomes true while $\overline{P}_0$ goes from true to false. This trailing edge opens the target gate through flip-flop a (Figs. 9b and 9c).[*]

The width register and counter is loaded on the "load 5"-pulse. While I_0 is true the counter is inhibited so that no counting can take place during the loading interval (Fig. 9d). When a goes true the counter starts counting down the pulse width on the trailing edges of the clock pulses d_3. After it reaches the count 1 and on the leading edge of the next clock pulse ω_0 goes true (Fig. 9e) and goes false again on its trailing edge. Thus the form of ω_0 is a single pulse on the trailing edge of which the flip-flop a is inverted resulting in the pulse width $\omega/32$ miles where ω is the number in the target width register. The output of flip-flop a is used to drive fast solid state switches in series with the 375 kHz CW.

2.   Target Phase Shift Generation (Fig. 1, block 5, Figs. 10 through 15)

The phase shift of the 375 kHz CW is generated in two stages from a digital 8-bit phase shift command coming from the computer. The first stage generates by digital techniques two square waves at roughly 20 kHz (precisely 5.1224375 MHz divided by $2^8 = 20009.52$ Hz) which are phase shifted with respect to each other by the required amount. The second stage generates from the above square waves by analog techniques two 375 kHz sine waves having the desired phase shift.

The first stage is illustrated in Fig. 10. The 8 bit phase shift command is loaded into registers A_1 through H_1 on the trailing edge of the "load-5"-pulse. The register is reset by the leading edge of the same pulse which coincides with the trailing edge of its inverse $\overline{L}_5$.

The circuits K through T form an exclusive OR from the variables at the left of the box symbol. For example, the Boolean output variable K equals $K = A\overline{A}_1 + \overline{A}A_1$. The

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[*] If the number loaded into the target range register is n, the distance of the leading edge of the pulse gate from the leading edge of the zero mile mark will be $(n+9)/64$ miles.

circuits A through J are very fast and different from the circuits used so far. All the inputs at the upper left of the circuit block are anded and, when the result is true, the state of the circuit is set to the value of the input at the lower left. Note that these circuits need a special clock pulse generated by the associated clock driver. Flip-flops A through H are connected as a counter. The output of H is a 5.1224375 MHz$/2^8$ square wave representing the reference signal. The outputs K through T of the exclusive OR circuits are true if $A \neq A_1$, $B \neq B_1$ ... etc.

Flip-flop J will flip on the clock pulse after K, L, M, N, P, R, and S are simultaneously true. H flips on the clock pulse after A through G are true (Fig. 11).

From the demand $K \cdot L \cdot M \cdot N \cdot P \cdot R \cdot S = 1$, we see that the 7-bit register A ... G must be the 1's complement of $A_1 ... G_1$ for a switch in J to occur. Counting in the A ... H register from the switch in J to the switch in H will therefore require the number of counts represented by the binary number in $A_1 ... G_1$. The switch in J will therefore precede the switch in H by the commanded phase angle.

So far we have said nothing about the direction in which the switches in H and J occur. If we ensure that the two square waves are in phase when $A_1 = B_1 = ... = H_1 = 0$ and in opposing phase when $A_1 = B_1 = ... = G_1 = 0$, $H_1 = 1$, any phase command will be executed correctly.

The left lower input to the flip-flop J is given by $\overline{T} \cdot \overline{J}$. Switching up will occur on the clock pulse after $\overline{T} \cdot \overline{J} = 1$ and $K \cdot L \cdot M \cdot N \cdot P \cdot R \cdot S = 1$. Switching down will occur on the clock pulse after $J = 1$ and $K \cdot L \cdot M \cdot N \cdot P \cdot R \cdot S = 1$. The condition $K \cdot L \cdot M \cdot N \cdot P \cdot R \cdot S = 1$ ensures that for zero phase or opposing phase switching of J occurs simultaneously with switching of H and need not be considered further.

For zero phase $H_1 = 0$; of course, before J has to switch up, $J = 0$. Hence for $H = 0$, $T = H\overline{H_1} + \overline{H}H_1 = 0$ and $\overline{T} = 1$. Since $\overline{J} = 1$, it follows that $\overline{T}\overline{J} = 1$ and J will indeed switch up. If J happens to be up when $\overline{T} = 1$, it will switch down, but on the next half cycle it cannot switch because then $H \neq H_1$ and $\overline{T} = 0$. The next switch up will occur on the next half cycle in phase with H. A similar consideration applies for the phase command 180° ($H_1 = 1$).

When the number in the phase register is changed a transient is produced in the output which will not exist for longer than 100 μsec. The phase of a target can be changed within one PRF interval.

A block diagram of the second analog circuit stage of the phase shift generator is given in Fig. 12. The 20 kHz square wave from the digital stage is fed through a band pass filter, amplified, and phase split (Fig. 13) for insertion into a carrier suppression modulator (Fig. 14).

The output of the modulator goes into a series narrow band rejection filter for further suppression of the lower sideband. After amplification the output is 375 kHz CW in phase with the incoming square wave. In the phase generator two of the above circuits are used, one for the reference signal and one for the phase shifted signal. The outputs from the phase shifter go to the pulse amplitude, width, and range generators.

The 20 kHz filter and amplifier (Fig. 12, block 1) are shown in Fig. 13. The amplification is controlled by the potentiometer P_1. The signal is then phase split in the GC 4 and the two signals, 180° apart in phase, are fed into cathode followers whose output impedances are sufficiently low to drive the balanced modulator. These signals then appear at the bases of the 2N1125 transistors in Fig. 14.

The amplifier in block 7 of Fig. 12 is illustrated in Fig. 15. Its amplification is controlled by the potentiometer P_2.

The output of the 355 kHz amplifier is fed to a cathode follower to adjust its impedance to that of the emitters of the 2N1255 transistors of the balanced modulators (Fig. 14). Two 2N1225 transistors of roughly equal characteristics were chosen in order to achieve optimum balance and carrier suppression. Moreover, the potentiometer P_3 serves as adjustment for this purpose. The collector voltage to the 2N1225 is supplied via the center tap of the carrier suppression LC network at a -30 volt level provided by the zener diode 1N3022 from a -135 volt source.

The carrier and lower side-band appear at the output better than 60 db lower than the 375 kHz upper side-band. The output voltage is approximately 1 volt.

Three meters monitor the 355 kHz and 20 kHz modulation input levels and the 375 kHz output signal levels. The test points allow the -135 and -30 V power supply voltages to be monitored.

3.   Target Pulse Switch and Amplitude Control (Fig. 1, blocks 8 and 9)

The target pulse switch and amplitude control connections are illustrated in Fig. 16. Both the 375 kHz CW reference and the phase shifted target signal are amplified and their level can be adjusted. The solid state switches 1 and 2 are actuated by their respective switch drivers which in turn are controlled by the flip-flop a (Fig. 9c).* The target pulse obtained is then attenuated in the binary relay attenuator which is commanded from the computer.

4.   Binary Attenuator (Fig. 1, block 6, Fig. 17)

The binary attenuator is composed of resistive symmetric π-sections matched to the characteristic impedance of the input and output cables. The sections are switched into or out of the circuit by fast relays. The change of amplitude is accomplished in 2-3 interpulse intervals. The relays are activated by a set of binary signals representing a binary number coming from the computer. Attenuations between 0 db and 63-3/4 db can be programmed in steps of 1/4 db. Figure 17 shows a circuit diagram of the attenuator. The bit connections on panel P_1 of Fig. 17 are connected to a set of relay drivers which in turn are connected to the flip-flops of the amplitude register. The latter is loaded from the computer on the trailing edge of the "load-5" command coming from the data circuits connect logic (Fig. 2).

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* Two switches are used in series in order to ensure sufficient rejection outside the gate.
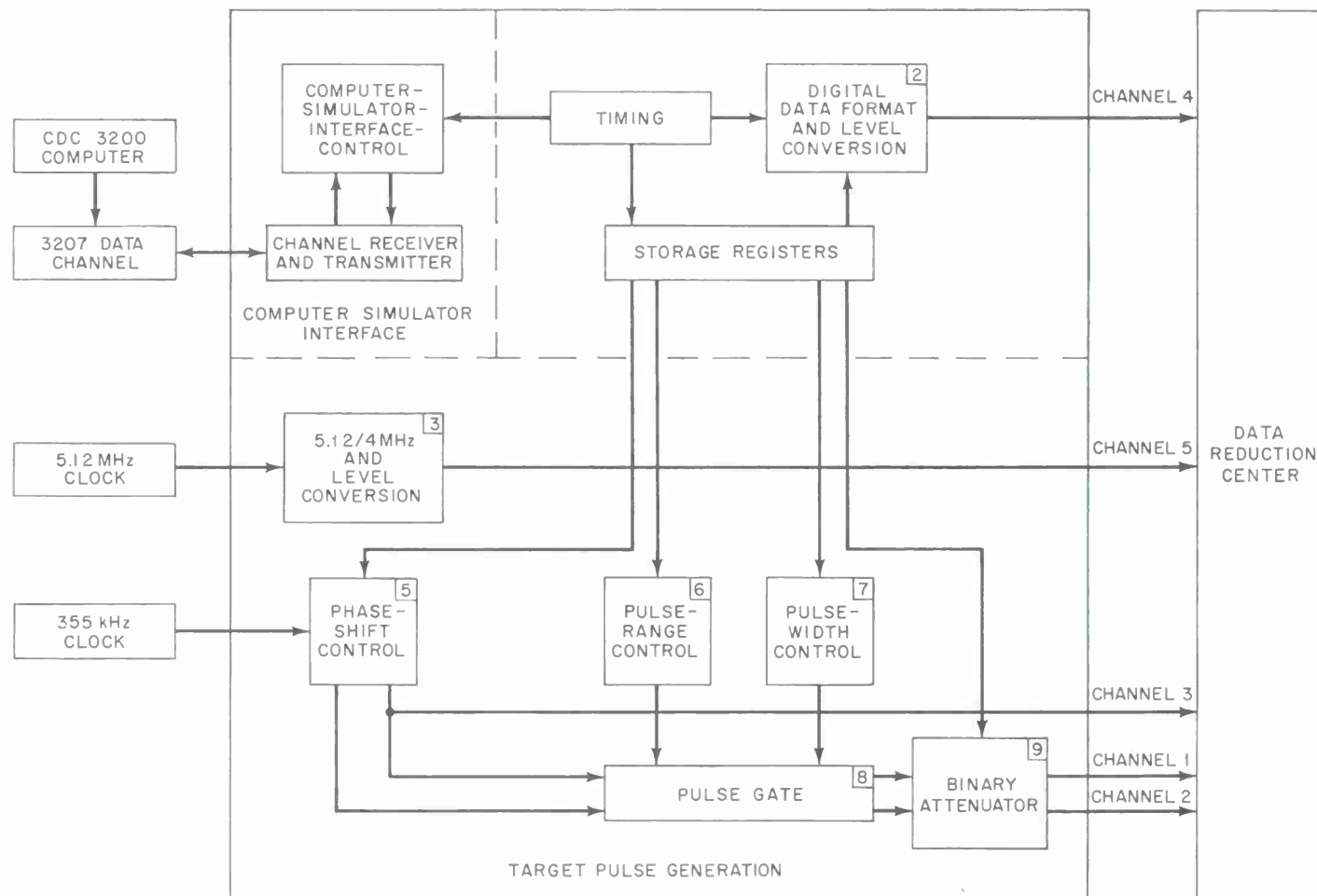
3-21-6467

CDC 3200 COMPUTER

3207 DATA CHANNEL

COMPUTER-SIMULATOR-INTERFACE-CONTROL

CHANNEL RECEIVER AND TRANSMITTER

COMPUTER SIMULATOR INTERFACE

TIMING

DIGITAL DATA FORMAT AND LEVEL CONVERSION [2]

CHANNEL 4

STORAGE REGISTERS

5.12 MHz CLOCK

5.12/4 MHz AND LEVEL CONVERSION [3]

CHANNEL 5

DATA REDUCTION CENTER

355 kHz CLOCK

PHASE-SHIFT CONTROL [5]

PULSE-RANGE CONTROL [6]

PULSE-WIDTH CONTROL [7]

CHANNEL 3

PULSE GATE [8]

BINARY ATTENUATOR [9]

CHANNEL 1

CHANNEL 2

TARGET PULSE GENERATION

Fig. 1.   Block diagram of the target simulator.

Fig. 2.   Data circuits connect logic.

14

3-21-6469
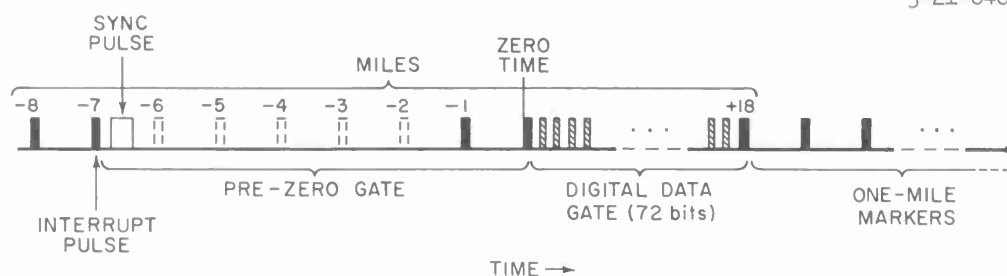
WIDTH OF THE SYNCH PULSE: 25 μsec

WIDTH OF THE OTHER PULSES: 6.247 μsec

TIME BETWEEN MILE MARKERS: 49.9762 μsec

THE PULSES DRAWN IN DASHED LINES ARE OMITTED

THE 72 POSITIONS FOR THE DATA BITS ARE OCCUPIED BY PULSES OR NOT,
 IF THE RESPECTIVE BIT IS ONE OR ZERO.

ONLY THE CROSSHATCHED PULSES ARE SIMULATED.

N.B. THIS FORMAT IS NOT YET FROZEN IN THE ABOVE FORM
      AND CHANGES ARE BEING APPLIED. THE CORRESPONDING
      CHANGE IN THE SIMULATOR FORMAT WILL BE REPORTED,
      WHEN THE FINAL MODIFICATIONS ARE MADE.
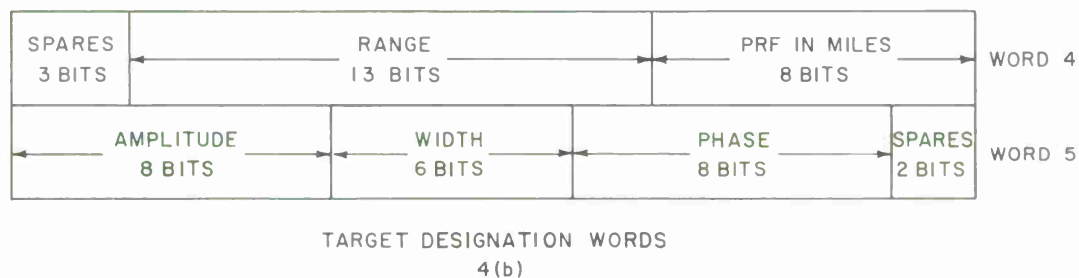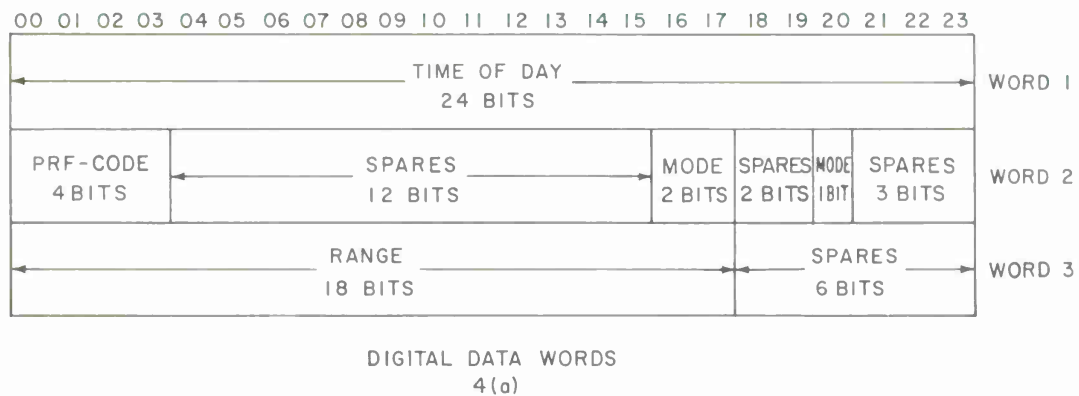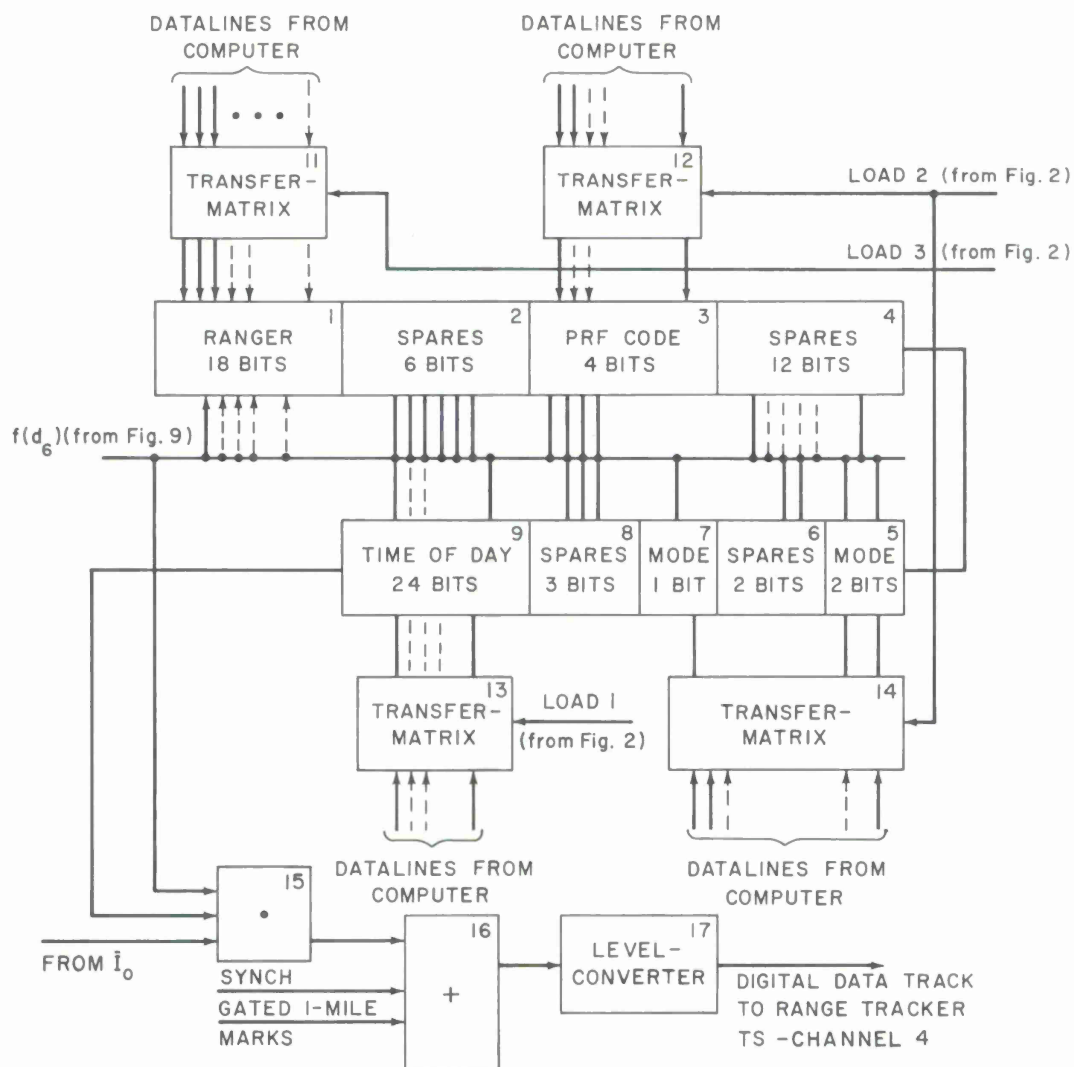
Fig. 3.   Digital data format.

00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23

TIME OF DAY 24 BITS		WORD 1

PRF-CODE 4 BITS	SPARES 12 BITS	MODE 2 BITS	SPARES 2 BITS	MODE 1 BIT	SPARES 3 BITS	WORD 2

RANGE 18 BITS	SPARES 6 BITS	WORD 3

DIGITAL DATA WORDS
4(a)

SPARES 3 BITS	RANGE 13 BITS	PRF IN MILES 8 BITS	WORD 4

AMPLITUDE 8 BITS	WIDTH 6 BITS	PHASE 8 BITS	SPARES 2 BITS	WORD 5

TARGET DESIGNATION WORDS
4(b)

Fig. 4. Word formats.

DATALINES FROM COMPUTER

DATALINES FROM COMPUTER

LOAD 2 (from Fig. 2)

LOAD 3 (from Fig. 2)

| 11 TRANSFER-MATRIX | 12 TRANSFER-MATRIX |

| 1 RANGER 18 BITS | 2 SPARES 6 BITS | 3 PRF CODE 4 BITS | 4 SPARES 12 BITS |

$f(d_6)$ (from Fig. 9)

| 9 TIME OF DAY 24 BITS | 8 SPARES 3 BITS | 7 MODE 1 BIT | 6 SPARES 2 BITS | 5 MODE 2 BITS |

| 13 TRANSFER-MATRIX | 14 TRANSFER-MATRIX |

LOAD 1 (from Fig. 2)

DATALINES FROM COMPUTER

DATALINES FROM COMPUTER

FROM $\bar{I}_o$

| 15 • |

SYNCH
GATED 1-MILE
MARKS

| 16 + |

| 17 LEVEL-CONVERTER |

DIGITAL DATA TRACK
TO RANGE TRACKER
TS -CHANNEL 4

Fig. 5.   Digital data formatting shift register.
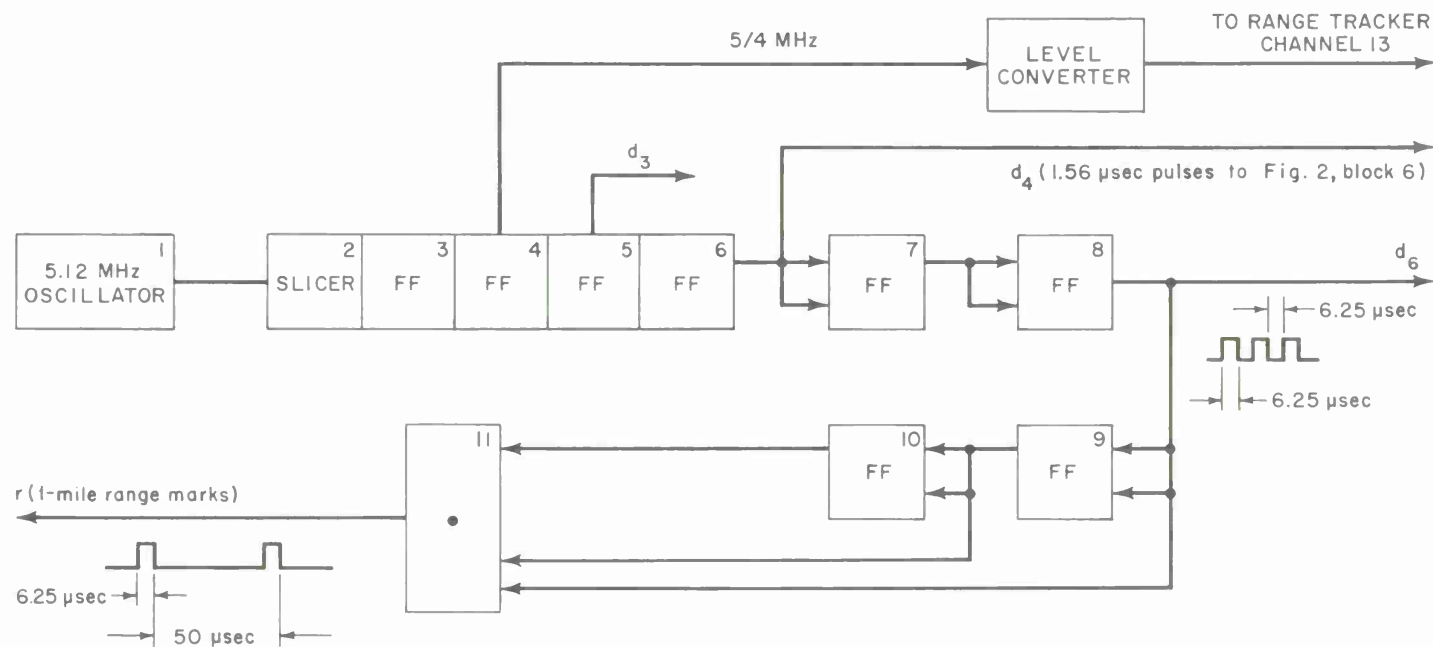
3-21-6472

Fig. 6.   One mile range mark generator.
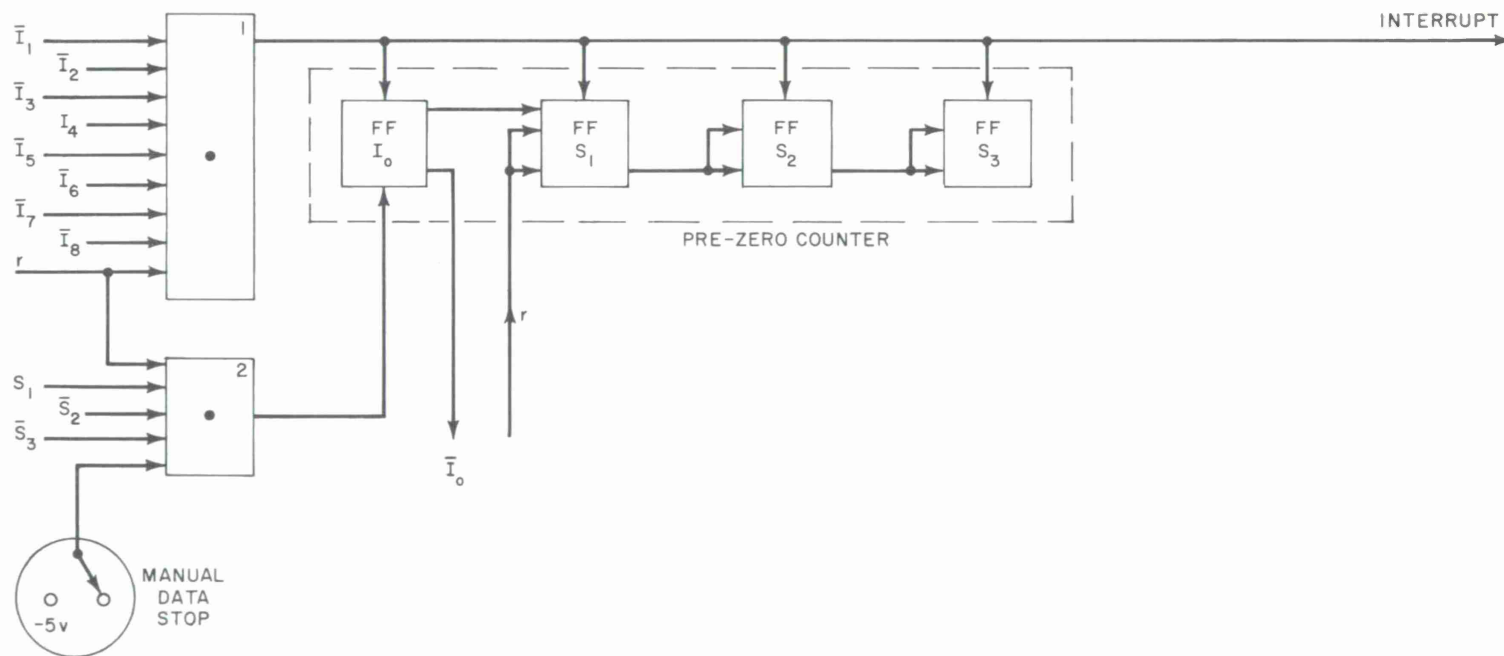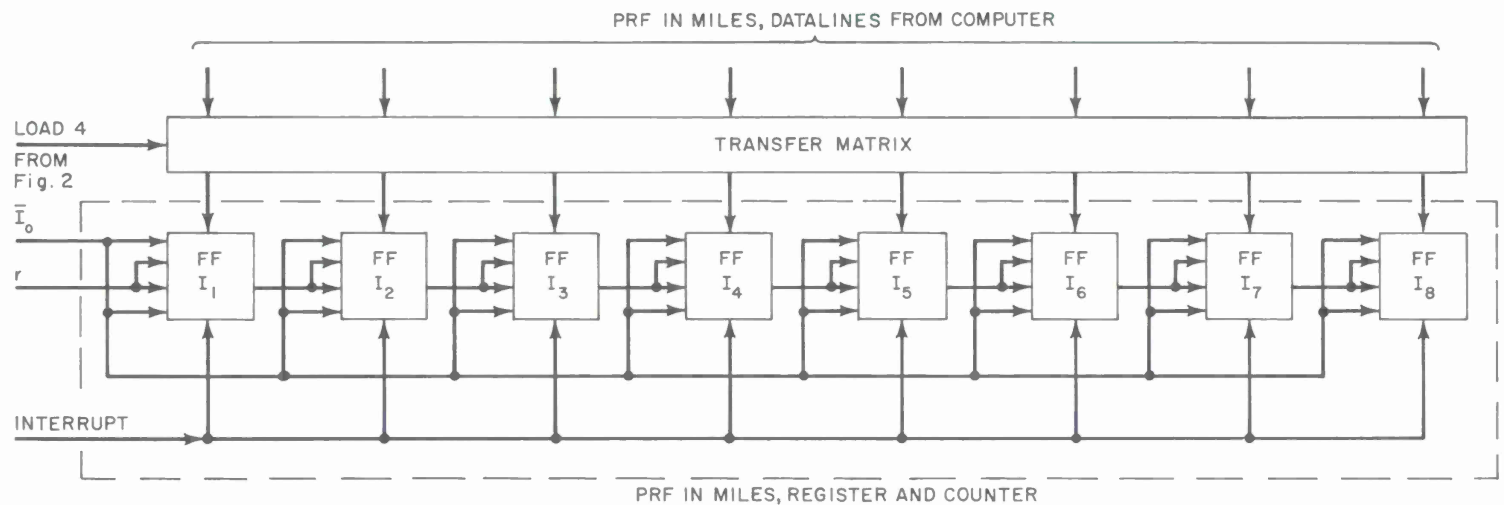
Fig. 7.   Interrupt generation.

19
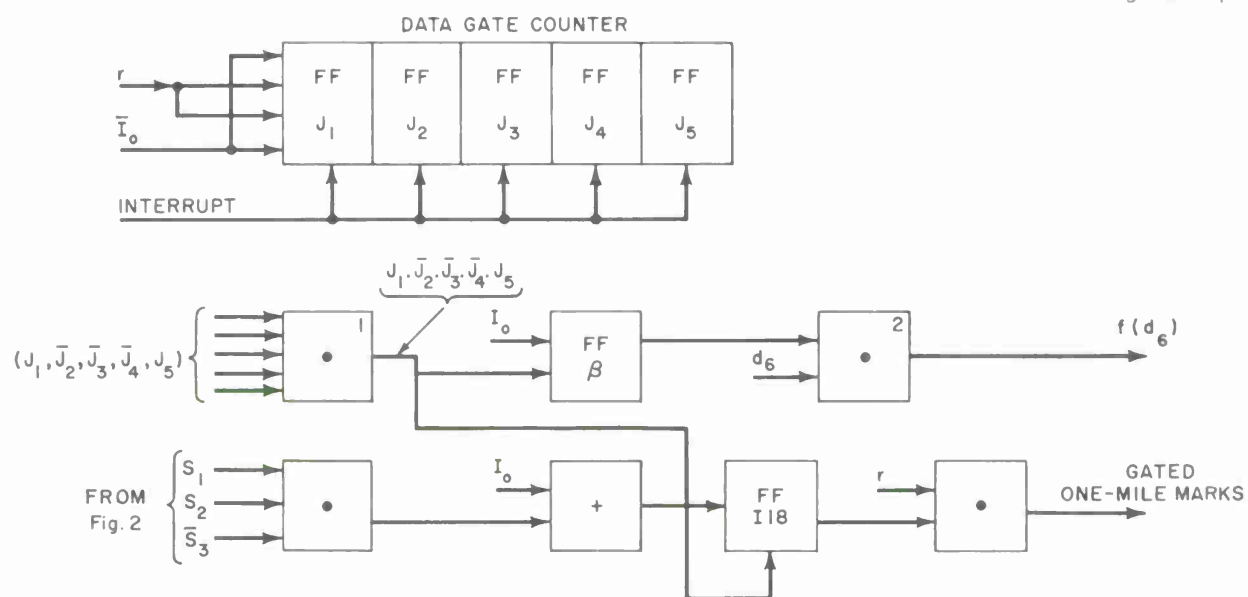
Fig. 8. Generation of the gated d_6 - pulses and gated one mile range marks.

TARGET RANGE, DATALINES FROM COMPUTER
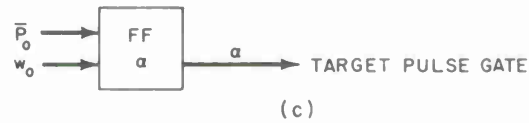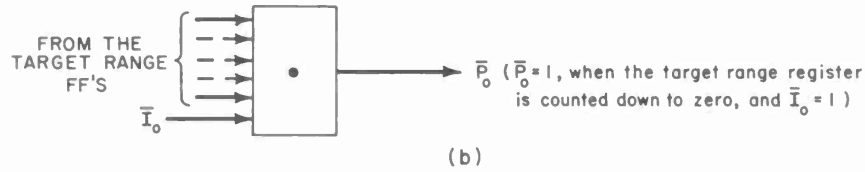
LOAD 4 (from Fig. 2) ────► **TARGET RANGE TRANSFER MATRIX**

$\bar{I}_0$

d_3

TARGET RANGE REGISTER AND COUNTER 13 BITS

I_0 ────►
w_0 ────► **F F I_p**

INTERRUPT

(a)

FROM THE TARGET RANGE FF'S

$\bar{I}_0$

────► $\bar{P}_0$ ($\bar{P}_0 = 1$, when the target range register is counted down to zero, and $\bar{I}_0 = 1$)

(b)

$\bar{P}_0$ ────►
w_0 ────► **FF α** ──α──► TARGET PULSE GATE

(c)

TARGET WIDTH, DATALINES FROM COMPUTER

LOAD 5 (from Fig. 2) ────► **WIDTH TRANSFER MATRIX**

d_3

$\bar{I}_0$

α ────► **WIDTH REGISTER AND COUNTER 6 BITS**

(d)

FROM THE TARGET WIDTH FF'S

d_3

────► w_0 ($w_0 = 1$, when the target width register is counted down to one, and $d_3 = 1$)

(e)

Fig. 9.   Target gate generation.
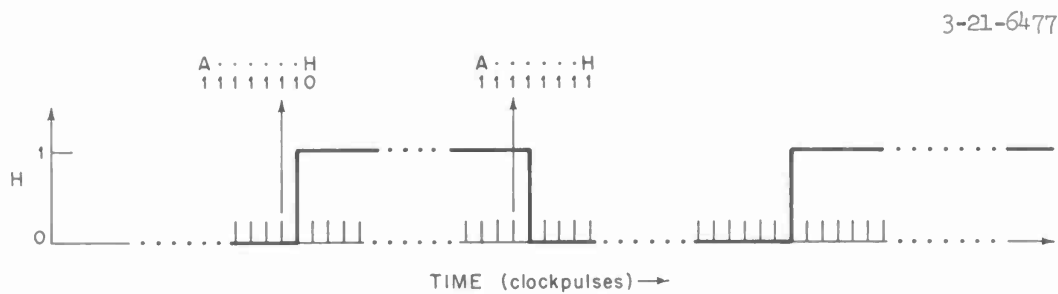
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Fig. 10.   Phaseshift generator digital circuits.

A · · · · · H
1 1 1 1 1 1 0

A · · · · · H
1 1 1 1 1 1 1

H

1

0

TIME (clockpulses) →

Fig. 11.   Switching times of flip-flop H.

| 20 kHz | FILTER AND AMPLIFIER | 1 | ~ | PHASE-SPLITTER | 2 | MODULATOR | 3 | 335 kHz BAND REJECTION FILTER | 4 | 375 kHz AMPLIFIER | 5 | 375 kHz CW |

| 355 kHz OSCILLATOR | 6 | 355 kHz AMPLIFIER | 7 | CATHODE FOLLOWER | 8 |
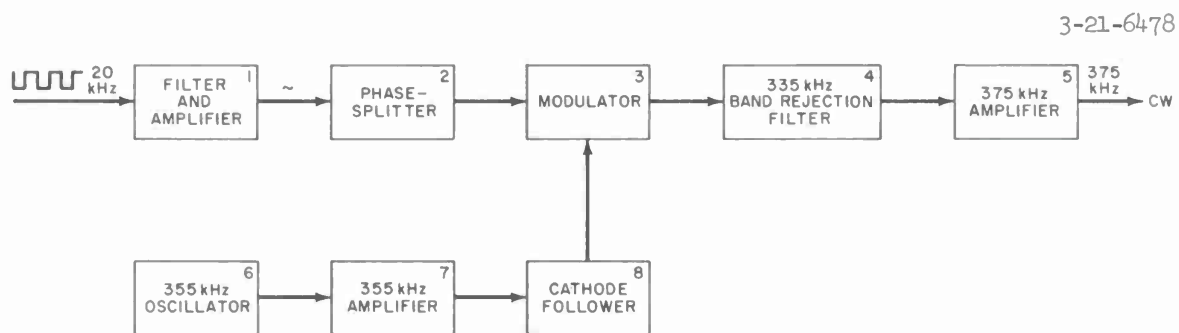
Fig. 12.   Phaseshift generator analog circuits.

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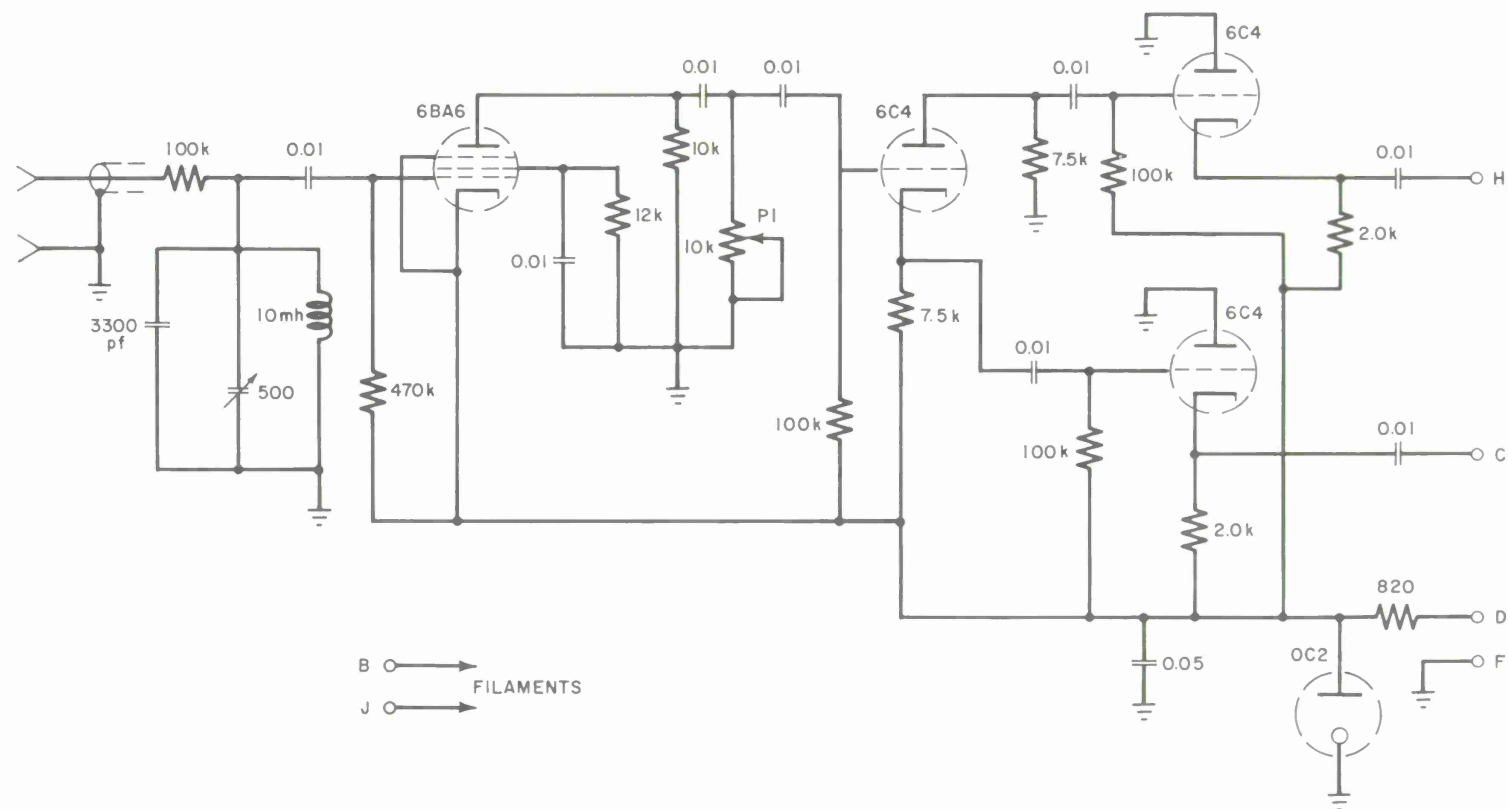
Fig. 13.   20 kHz filter and amplifier.
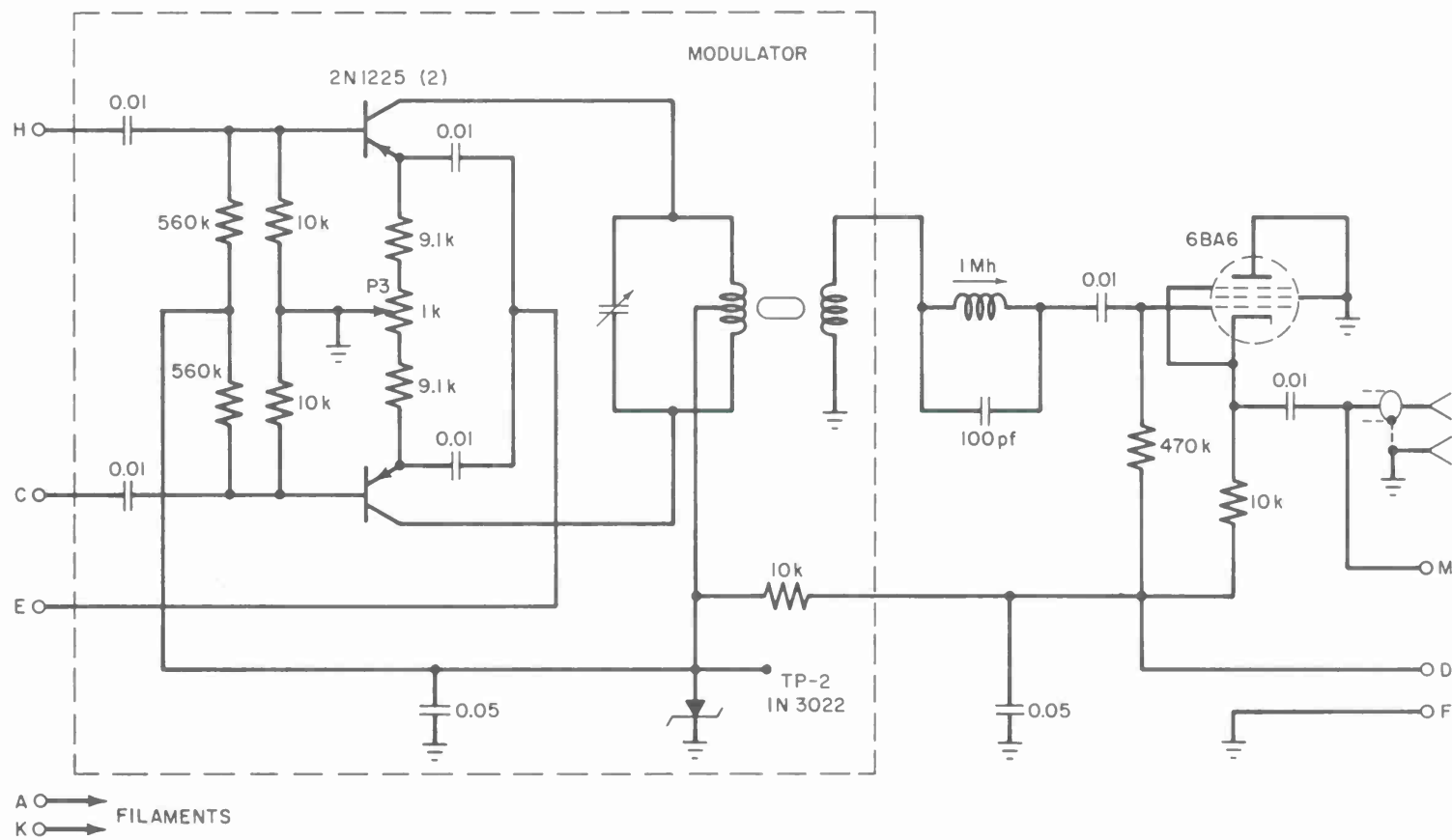
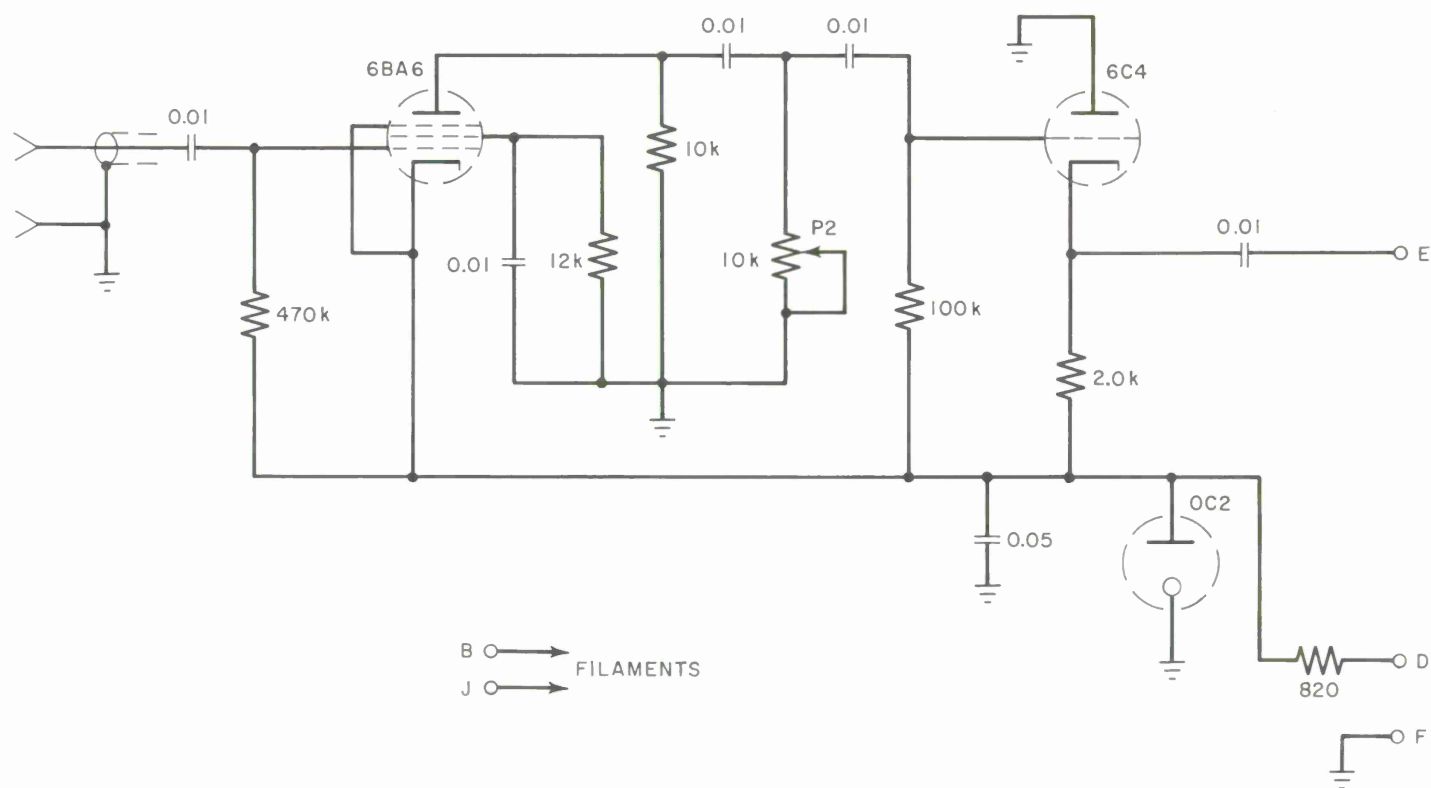Fig. 14.   Phaseshift generator modulator and band rejection filter.

355 kHz AMPLIFIER

Fig. 15.   kHz 355 amplifier.

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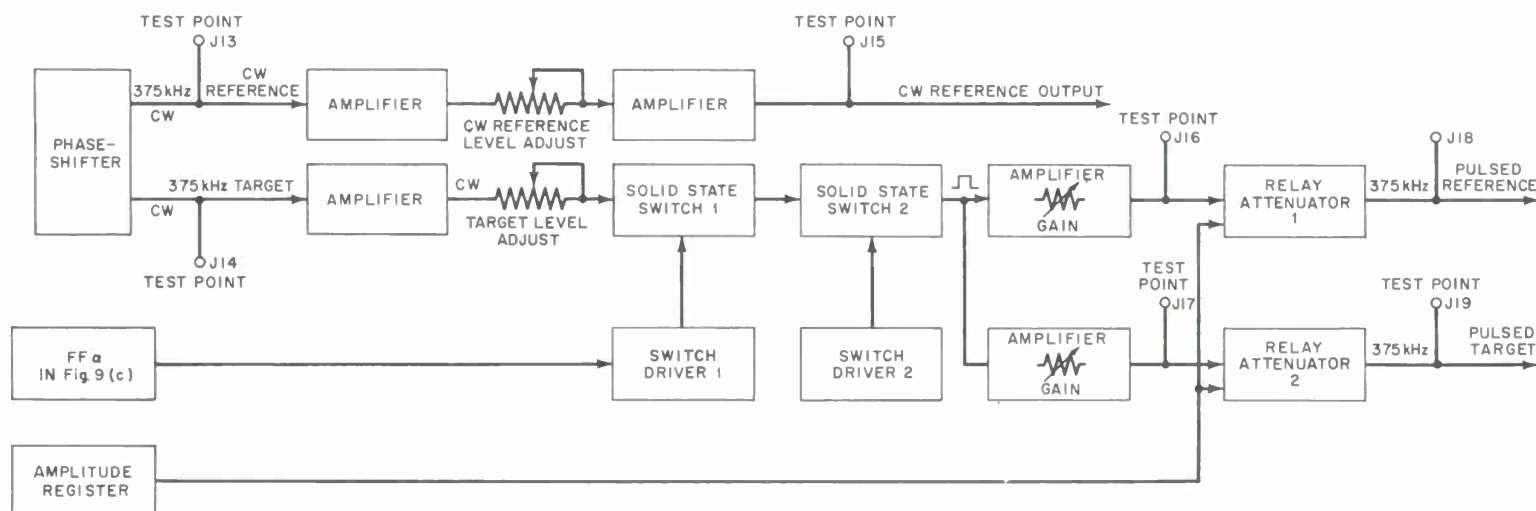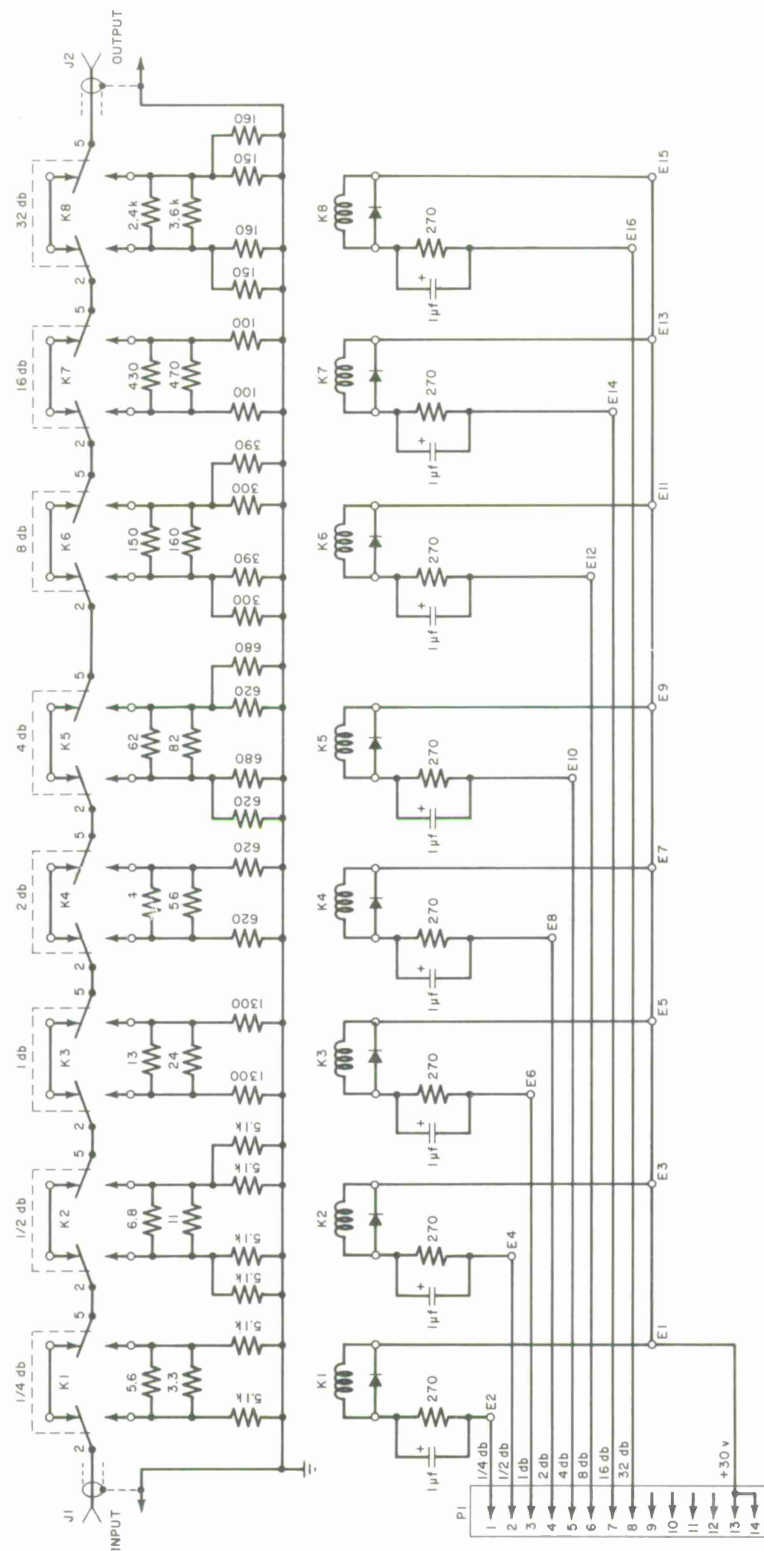Fig. 16.   Target pulse switch and amplitude control.

Fig. 17. Relay attenuator.

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13. ABSTRACT

It is very important for the operation of the Lincoln Data Recovery Center to be able to inject into it artificially generated targets. These target-pulses must simulate as closely as possible those appearing in the input from the I.F. tape into the D.R.C. and should be controllable in range, width, amplitude, phase and repetition rate by special computer programs written for the CDC-3200 computer. In addition to the FM channels of the tape, its digital channels must be simulated.

A target simulator has been constructed to the above specifications and is described in the text.

14. KEY WORDS

data processing
target simulator
CDC-3200

L-band
digital computers
flip-flops